UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,521	03/23/2004	Won-Jin Kim	5649-1226	2748

7590 02/22/2006

Laura M. Kelley
Myers Bigel Sibley & Sajovec, P.A.
P.O. Box 37428
Raleigh, NC 27627

EXAMINER	
LINDSAY JR, WALTER LEE	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 02/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

HA

Office Action Summary	Application No.	Applicant(s)	
	10/806,521	KIM ET AL.	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,15,23 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11,12 and 15* is/are allowed.

6)☒ Claim(s) *1 and 9* is/are rejected.

7)☒ Claim(s) *2-8,10,23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to a Response filed on 12/12/05.

Currently, claims 1-12, 15 and 23-24 are pending.

Specification

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Ota et al. (U.S. Patent No. 6,861,359 filed 5/20/2003).

Ota shows the method as claimed in Figs. 2A-2F and corresponding text as: forming at least one layer on a first and a second side of a semiconductor substrate (1); removing portions of the least one layer (5) on the first side of the semiconductor substrate to form a pattern of the least one layer on the first side of the substrate while maintaining the at least one layer on the second side of the substrate (col. 5, line 34-

col. 6, line 40); forming a capping layer (4) on the pattern of the at least one layer on the first side of the substrate and on the at least one layer on the second side of the semiconductor substrate (col. 5, line 34- col. 6, line 40); removing the capping layer (4) on the second side of the semiconductor substrate thereby exposing the at least one layer on the second side of the substrate while maintaining the capping layer on the first side of the substrate (col. 6, lines 22-32); removing the at least one layer on the second side of the semiconductor substrate, while maintaining the capping layer and the pattern of the at least one layer on the first side of the semiconductor substrate (col. 6, lines 22-32); and removing a portion of the capping layer on the first side of the semiconductor substrate (col. 6, lines 33-40) (claim 1). Ota teaches removing the capping layer on substantially the entire second side of the semiconductor substrate (col. 6, lines 22-32) (claims 9).

Allowable Subject Matter

4. Claims 2-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 11-12, 15 and 23-24 are allowed.

6. The following is an examiner's statement of reasons for allowance: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...wherein removing the at least one layer on the second side of the semiconductor substrate precedes removing a portion of the capping layer on the first side of the semiconductor substrate, as required by claim 11; and

...forming a conductive layer on the gate pattern and on the first side of the substrate and on the masking layer on the second side of the semiconductor substrate;

removing the conductive layer on the second side of the semiconductor substrate thereby exposing the masking layer;

removing the masking layer, the gate electrode layer and the gate insulating layer on the second side of the semiconductor substrate while maintaining the conductive layer and the gate pattern on the first side of the semiconductor substrate; and

removing a portion of the conductive layer on the first side of the semiconductor substrate to form contact pads between portions of the gate pattern, as required by claim 15.

removing a portion of the conductive layer on the first side of the semiconductor substrate to form contact pads between portions of the gate pattern,.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL
February 14, 2006